



COMPUTER ORGANIZATION AND ARCHITECTURE (CS304PC) COURSE PLANNER

I. COURSE OVERVIEW:

1	To know the background of internal communication of computer
2	To have better idea on how to write assemble language programs
3	To be clear with memory management techniques
4	To better with IO devices communication with processor
5	To notice how to perform computer arithmetic operations
6	To be clear with pipeline procedure and multi processors.

II. PREREQUISITE:

1. Digital Logic Design

III. COURSE OBJECTIVES:

1	The purpose of the course is to introduce principles of computer organization and the basic architectural concepts.
2	It begins with basic organization, design, and programming of a simple digital computer and introduces simple register transfer language to specify various computer operations.
3	Topics include computer arithmetic, instruction set design, micro programmed control unit, pipelining and vector processing, memory organization and I/O systems, and multiprocessors

IV. COURSE OUTCOMES:

After completing this course the student must demonstrate the knowledge and ability to:

S.No	Description	Bloom's Taxonomy Level
1	Understand the basics of instructions sets and their impact on processor design	L2: Understand
2	Demonstrate an understanding of the design of the functional units of a digital computer system.	L3 : Application
3	Evaluate cost performance and design trade-offs in designing and constructing a computer processor including memory.	L3 : Application
4	Design a pipeline for consistent execution of instructions with minimum hazards	L5 : Synthesize
5	Manipulate representations of numbers stored in digital computers	L3 : Application



V. HOW PROGRAM OUTCOMES ARE ASSESSED:

Program Outcomes (PO)		Level	Proficiency assessed by
PO1	Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems related to Computer Science and Engineering.	3	Assignment Mock test Quiz
PO2	Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems related to Computer Science and Engineering and reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.	3	Assignment Mock test Quiz
PO3	Design/development of solutions: Design solutions for complex engineering problems related to Computer Science and Engineering and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.	3	Assignment Mock test Quiz
PO4	Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	3	Assignment Mock test Quiz
PO5	Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.	3	Mini Project
PO6	The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the Computer Science and Engineering professional engineering practice.	1	Quiz
PO7	Environment and sustainability: Understand the impact of the Computer Science and Engineering professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.	2	Quiz
PO8	Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.	-	-
PO9	Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.	3	Quiz



PO1 0	Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.	-	-
PO1 1	Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.	-	-
PO1 2	Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.	3	Competitive Examinations

1:Slight(Low) 2:Moderate(Medium) 3:Substantial(High) - :None

- End-of-course surveys (Quarterly).
- Instructor evaluation reports (Quarterly).
- Department performance report (Quarterly).
- Student exit survey (Yearly).
- Alumni survey (Yearly).
- Alumni Advisory Board (Once or twice yearly).
- Student Advisory Committee (Once or twice yearly).

VI. HOW PROGRAM SPECIFIC OUTCOMES ARE ASSESSED:

Program Specific Outcomes (PSO)		Level	Proficiency assessed by
PSO1	Foundation of mathematical concepts: To use mathematical methodologies to crack problem using suitable mathematical analysis, data structure and suitable algorithm.	3	Technical Paper Writing
PSO2	Foundation of Computer System: The ability to interpret the fundamental concepts and methodology of computer systems. Students can understand the functionality of hardware and software aspects of computer systems.	3	Slip Test
PSO3	Foundations of Software development: The ability to grasp the software development lifecycle and methodologies of software systems. Possess competent skills and knowledge of software design process. Familiarity and practical proficiency with a broad area of programming concepts and provide new ideas and innovations towards research.	2	Research oriented Studies

VII. SCOPE OF COURSE:

At the end of the course the student would:

1. Ability to understand basic structure of computer.
2. Ability to perform computer arithmetic operations.
3. Ability to understand control unit operations.
4. Ability to understand the concept of cache mapping techniques.



5. Ability to understand the concept of I/O organization.
6. Ability to conceptualize instruction level parallelism

VIII. SYLLABUS:

UNIT - I

Digital Computers: Introduction, Block diagram of Digital Computer, Definition of Computer Organization, Computer Design and Computer Architecture.

Register Transfer Language and Micro operations: Register Transfer language, Register Transfer, Bus and memory transfers, Arithmetic Micro operations, logic micro operations, shift micro operations, Arithmetic logic shift unit.

Basic Computer Organization and Design: Instruction codes, Computer Registers Computer instructions, Timing and Control, Instruction cycle, Memory Reference Instructions, Input – Output and Interrupt.

UNIT - II

Microprogrammed Control: Control memory, Address sequencing, micro program example, design of control unit.

Central Processing Unit: General Register Organization, Instruction Formats, Addressing modes, Data Transfer and Manipulation, Program Control.

UNIT - III

Data Representation: Data types, Complements, Fixed Point Representation, Floating Point Representation.

Computer Arithmetic: Addition and subtraction, multiplication Algorithms, Division Algorithms, Floating – point Arithmetic operations. Decimal Arithmetic unit, Decimal Arithmetic operations.

UNIT - IV

Input-Output Organization: Input-Output Interface, Asynchronous data transfer, Modes of Transfer, Priority Interrupt Direct memory Access.

Memory Organization: Memory Hierarchy, Main Memory, Auxiliary memory, Associate Memory, Cache Memory.

UNIT - V

Reduced Instruction Set Computer: CISC Characteristics, RISC Characteristics.

Pipeline and Vector Processing: Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, RISC Pipeline, Vector Processing, Array Processor.

Multi Processors: Characteristics of Multiprocessors, Interconnection Structures, Interprocessor arbitration, Interprocessor communication and synchronization, Cache Coherence.

TEXT BOOK:

1. Computer System Architecture – M. Moris Mano, Third Edition, Pearson/PHI.

REFERENCES:

- 1.Computer Organization – Car Hamacher, Zvonks Vranesic, Safea Zaky, Vth Edition, McGraw Hill.
- 2.Computer Organization and Architecture – William Stallings Sixth Edition,Pearson/PHI.
- 3.Structured Computer Organization – Andrew S. Tanenbaum, 4th Edition,PHI/Pearson.



IX. LESSON PLAN-COURSE SCHEDULE:

S.No	Unit	Topics To be Covered	Link for PPT	Link for PDF	Course Learning Outcome	Teaching Aids	Text Book
1	I	Digital Computers: Introduction	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Define a Computer	BB, PPT	T1
2		Block diagram of Digital Computer	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Discuss about the Block Diagram of a Computer	BB, PPT	T1
3		Definition of Computer Organization, Computer Design and Computer Architecture.	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Define CO,CA and CD	BB, PPT	T1
4		Register Transfer Language and Micro operations: Register Transfer language, Register Transfer	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Discuss about RTL	BB, PPT	T1
5		Bus and memory transfers	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Discuss about bus ,memory transfers	BB, PPT	T1
6		Arithmetic	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain	BB, PPT	T1



		Micro operations	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Arithmetic Micro operations		
7		Arithmetic Micro operations	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain Arithmetic Micro operations	BB, PPT	T1
8		logic micro operations	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain logic micro operations	BB, PPT	T1
9		logic micro operations	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain logic micro operations	BB, PPT	T1
10		shift micro operations	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain shift micro operations	BB, PPT	T1
11		shift micro operations	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain shift micro operations	BB, PPT	T1
12		Arithmetic logic shift unit.	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain ALU	BB, PPT	T1



13	Arithmetic logic shift unit.	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain ALU	BB, PPT	T1
14	Basic Computer Organization and Design: Instruction codes,	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	List Computer Registers	BB, PPT	T1
15	Computer Registers	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	List Computer Registers	BB, PPT	T1
16	Computer instructions	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain computer instructions	BB, PPT	T1
17	Timing and Control	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Discuss Timing And Control	BB, PPT	T1
18	Instruction cycle	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Define Instruction Cycle	BB, PPT	T1
19	Memory Reference Instructions,	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain memory and I/O instructions	BB, PPT	T1



			LB4j0jZ6Me				
20		Input – Output and Interrupt.	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain I/O Interrupt	BB, PPT	T1
21	II	Microprogrammed Control: Control memory,	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Discuss different terminology in MPU	BB, PPT	T1
22		Address sequencing	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Discuss Address Sequencing Tech.	BB, PPT	T1
23		Micro program example	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Write example micro programs	BB, PPT	T1
24		Micro program example	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Write example micro programs	BB, PPT	T1
25		Design of control unit.	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Design control unit	BB, PPT	T1
26		Design of control unit.	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Design control unit	BB, PPT	T1



			p1Lmd1fn6x9LB4j0jZ6Me	Me			
27		Central Processing Unit: General Register Organization,	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Discuss Register Org	BB, PPT	T1
28		** Stack Organization	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Discuss Stack Org	BB, PPT	T1
29		Instruction Formats: Three Address Instructions, Two Address Instructions	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain Instruction Formats	BB, PPT	T1
30		Instruction Formats : One Address Instructions, Zero Address Instructions	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain Instruction Formats	BB, PPT	T1
31		Addressing modes	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain Addressing mode of operation	BB, PPT	T1
32		Addressing modes	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain Addressing mode of operation	BB, PPT	T1
33		Data Transfer and	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain Data Transfer and	BB, PPT	T1



		Manipulation	ve/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	s/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Manipulation		
34		Data Transfer and Manipulation	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folder/s/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain Data Transfer and Manipulation	BB, PPT	T1
35		Program Control.	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folder/s/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Define Program Control.	BB, PPT	T1
36		Program Control.	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folder/s/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Define Program Control.	BB, PPT	T1
37	III	Data Representation: Data types	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folder/s/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain data representation	BB, PPT	T1
38		Complements (r-1)'s Complement and (r's Complement)	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folder/s/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain 1's and r's complement with example	BB, PPT	T1
39		Fixed Point Representation,	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folder/s/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain Fixed Point Representation,	BB, PPT	T1
40		Fixed Point	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folder/s/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain Fixed	BB, PPT	T1



		Representatio n,	oogle.com/dri ve/u/1/folders/ 1Iz2x69Zvlnn p1Lmd1fn6x9 LB4j0jZ6Me	com/drive/u/1/folder s/1Iz2x69Zvlnnp1L md1fn6x9LB4j0jZ6 Me	Point Representation,		
41		Floating Point Representatio n.	https://drive.g oogle.com/dri ve/u/1/folders/ 1Iz2x69Zvlnn p1Lmd1fn6x9 LB4j0jZ6Me	https://drive.google. com/drive/u/1/folder s/1Iz2x69Zvlnnp1L md1fn6x9LB4j0jZ6 Me	Explain Floating Point Representation.	BB, PPT	T1
42		Computer Arithmetic: Addition and subtraction	https://drive.g oogle.com/dri ve/u/1/folders/ 1Iz2x69Zvlnn p1Lmd1fn6x9 LB4j0jZ6Me	https://drive.google. com/drive/u/1/folder s/1Iz2x69Zvlnnp1L md1fn6x9LB4j0jZ6 Me	Explain computer arithmetic operations	BB, PPT	T1
43		Computer Arithmetic: Addition and subtraction	https://drive.g oogle.com/dri ve/u/1/folders/ 1Iz2x69Zvlnn p1Lmd1fn6x9 LB4j0jZ6Me	https://drive.google. com/drive/u/1/folder s/1Iz2x69Zvlnnp1L md1fn6x9LB4j0jZ6 Me	Explain computer arithmetic operations	BB, PPT	T1
44		Multiplicatio n Algorithms	https://drive.g oogle.com/dri ve/u/1/folders/ 1Iz2x69Zvlnn p1Lmd1fn6x9 LB4j0jZ6Me	https://drive.google. com/drive/u/1/folder s/1Iz2x69Zvlnnp1L md1fn6x9LB4j0jZ6 Me	Design multiplication algorithm	BB, PPT	T1
45		Multiplicatio n Algorithms	https://drive.g oogle.com/dri ve/u/1/folders/ 1Iz2x69Zvlnn p1Lmd1fn6x9 LB4j0jZ6Me	https://drive.google. com/drive/u/1/folder s/1Iz2x69Zvlnnp1L md1fn6x9LB4j0jZ6 Me	Design multiplication algorithm	BB, PPT	T1
46		Division Algorithms	https://drive.g oogle.com/dri ve/u/1/folders/ 1Iz2x69Zvlnn p1Lmd1fn6x9 LB4j0jZ6Me	https://drive.google. com/drive/u/1/folder s/1Iz2x69Zvlnnp1L md1fn6x9LB4j0jZ6 Me	Design multiplication algorithm	BB, PPT	T1



47		Division Algorithms	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Design division algorithm	BB, PPT	T1
48		Floating – point Arithmetic operations.	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain floating point arithmetic	BB, PPT	T1
49		Floating – point Arithmetic operations.	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain floating point arithmetic	BB, PPT	T1
50		Decimal Arithmetic unit	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain DAU	BB, PPT	T1
51		Decimal Arithmetic unit	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain DAU	BB, PPT	T1
52	IV	Input-Output Organization: Input-Output Interface	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Define IOI	BB, PPT	T1
53		Asynchronous data transfer	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Discuss Asynchronous Data	BB, PPT	T1



			LB4j0jZ6Me				
54		Modes of Transfer	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain Modes of transfer	BB, PPT	T1
55		Priority Interrupt	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain Priority Interrupt	BB, PPT	T1
56		Direct memory Access.	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain DMA	BB, PPT	T1
57		Discuss Memory Hierarchy, Main Memory	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain Main Memory, Discuss Memory Hierarchy	BB, PPT	T1
58		Auxiliary memory	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain Auxiliary memory	BB, PPT	T1
59		Associate Memory	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain Associate Memory	BB, PPT	T1
60		Cache Memory	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain Cache Memory	BB, PPT	T1



			p1Lmd1fn6x9LB4j0jZ6Me	Me			
61	V	Reduced Instruction Set Computer: CISC Characteristic s,	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lp1Lmd1fn6x9LB4j0jZ6Me	Define RISC & CISC	BB, PPT	T1
62		RISC Characteristic s.	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lp1Lmd1fn6x9LB4j0jZ6Me	Difference btw RISC & CISC	BB, PPT	T1
63		Pipeline and Vector Processing:	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lp1Lmd1fn6x9LB4j0jZ6Me	Expain Pipeline and Vector Processing	BB, PPT	T1
64		Parallel Processing,	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lp1Lmd1fn6x9LB4j0jZ6Me	discuss about Parallel Processing	BB, PPT	T1
65		Pipelining, Arithmetic Pipeline,	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lp1Lmd1fn6x9LB4j0jZ6Me	Explain pipelining types	BB, PPT	T1
66		Instruction Pipeline,	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lp1Lmd1fn6x9LB4j0jZ6Me	Explain pipelining types	BB, PPT	T1
67		RISC Pipeline,	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lp1Lmd1fn6x9LB4j0jZ6Me	Explain pipelining types	BB, PPT	T1



			ve/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	s/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me			
68		Vector Processing,	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folder/s/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain Vector Processing	BB, PPT	T1
69		Array Processor	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folder/s/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain Vector Processing	BB, PPT	T1
70		Multi Processors: Characteristics of Multiprocessors,	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folder/s/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain Characteristics of Multiprocessor	BB, PPT	T1
71		Interconnection Structures,	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folder/s/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Explain Interconnection Structures	BB, PPT	T1
72		Inter - Processor arbitration,	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folder/s/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Define Inter - Processor arbitration	BB, PPT	T1
73		Inter - Processor communication and synchronization,	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folder/s/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Define IPC And Synchronization	BB, PPT	T1
74		Cache	https://drive.google.com/drive/u/1/folders/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	https://drive.google.com/drive/u/1/folder/s/1Iz2x69Zvlnnp1Lmd1fn6x9LB4j0jZ6Me	Discuss about	BB, PPT	T1



		Coherence.	oogole.com/dri ve/u/1/folders/ 1Iz2x69Zvlnn p1Lmd1fn6x9 LB4j0jZ6Me	com/drive/u/1/folder s/1Iz2x69Zvlnnp1L md1fn6x9LB4j0jZ6 Me	Cache Coherence Prob.		
--	--	------------	---	---	--------------------------	--	--

X. MAPPING COURSE OUTCOMES LEADING TO THE ACHIEVEMENT OF PROGRAM OUTCOMES AND PROGRAM SPECIFIC OUTCOMES:

	Program Outcomes												Program Specific Outcomes		
	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
CO1	3	3	-	-	3	-	2	-	-	-	-	2	2	3	2
CO2	3	3	-	3	2	-	-	-	-	-	-	-	3	3	2
CO3	3	3	-	3	2	-	2	-	-	-	-	-	3	3	2
CO4	3	2	3	2	-	-	2	-	-	-	-	-	3	2	1
CO5	3	3	3	-	2	-	-	-	3	-	-	-	3	3	1
AVG	3.00	2.80	3.00	2.67	2.25	0.00	2.00	0.00	3.00	0.00	0.00	2.00	2.80	2.80	1.60

DESCRIPTIVE QUESTIONS:

UNIT-I

Short Answer Questions-

S.NO	QUESTION	BLOOMS Taxonomy	Course Outcome
1.	Define Computer Architecture?	L1:Remember	CO2
2.	Define a Digital Computer ? Draw block diagram of Computer.	L1:Remember	CO2
3.	What is the need of Register? Explain the different types of Registers.	L1:Understand	CO3
4.	What is control memory?	L1:Understand	CO3
5.	Define a Micro Program & Micro Instruction?	L1:Remember	CO2

Long Answer Questions-

S.NO	QUESTION	BLOOMS Taxonomy	Course Outcome
1.	How to do address sequencing with diagram.	L2:Understand	CO4
2.	What is instruction format? Explain the different instruction formats in detail.	L2:Understand	CO3



3.	Explain the different phases of Instruction Cycle?	L2:Understand	CO4
4.	Explain the Micro Program Control with Diagram & Examples?	L2:Understand	CO4
5.	List out any 5 Registers with explains in detail.	L1:Remember	CO5
6.	Demonstrate the Three – State Bus Buffer with neat diagram	L2:Understand	CO3
7.	List and Explain in detail about the memory reference Instructions	L1:Remember	CO5
8.	Draw the flowchart for interrupt cycle and experiment with it with explanation	L3:Applying	CO4
9.	Determine the input-output configuration	L5: Evaluating	CO3
10.	Explain the stored program organization with neat diagram	L2:Understand	CO3

UNIT-2

Short Answer Questions

S.NO	QUESTION	BLOOMS Taxonomy	Course Outcome
1.	Define Data path.	L1:Remember	CO2
2.	Define Latency and throughput	L1:Remember	CO2
3.	Discuss the principle operation of micro programmed control unit.	L2:Understand	CO1
4.	What is control store?	L2:Understand	CO3
5.	Define Processor clock.	L1:Remember	CO2

Long Answer Questions-

S.NO	QUESTION	BLOOMS Taxonomy	Course Outcome
1.	Draw and explain typical hardware control unit.	L2:Understand	CO4
2.	Draw and explain about micro program control unit.	L2:Understand	CO4
3.	Write short notes on (i)Micro instruction format (ii) Symbolic micro instruction.	L2:Understand	CO1
4.	Explain multiple bus organization	L2:Understand	CO3



	in detail.		
5.	Explain in detail about conditional branching with neat diagram	L2: Understand	CO3
6.	Explain general register organization in detail with neat diagrams	L2: Understand	CO3
7.	**Explain Stack organization in detail with neat diagrams	L2: Understand	CO3
8.	Evaluate the following program using three address Instruction format $X = (A+B) * (C+D)$	L5: Evaluate	CO2
9.	Evaluate the following program using two address Instruction format $X = (A+B) * (C+D)$	L5: Evaluate	CO2
10.	Evaluate the following program using one address Instruction format $X = (A+B) * (C+D)$	L5: Evaluate	CO2

UNIT-3

Short Answer Questions-

S.NO	QUESTION	BLOOMS Taxonomy	Course Outcome
1.	Convert the following decimal number to the base indicated a. 7562 to octal b. 1938 to hexadecimal	L5: Evaluate	CO4
2.	Find the 1's and 2's complement of the following eight digit binary number a. 10101110 b. 10000001	L1: Remember	CO1
3.	List the steps of Booth's Multiplication algorithm	L4: Analyze	CO3
4.	Convert the following decimal number to the base indicated a. 17562 to octal b. 11938 to hexadecimal	L5: Evaluate	CO1
5.	Briefly explain r's complement with example	L2: Understand	CO2



Long Answer Questions-

S.NO	QUESTION	BLOOMS Taxonomy	Course Outcome
1.	Draw and explain the hardware for signed – magnitude addition and subtraction.	L2:Understand	CO3
2.	Explain the booth's multiplication algorithm with neat sketch of hardware design	L6:Design	CO4
3.	Perform division of 1000 and 0011 using restoring division algorithm.	L5:Evaluate	CO2
4.	Multiply 7 and 3 using Booth's algorithm.	L4:Analyse	CO1
5.	Draw a flowchart for adding and subtracting two fixed point binary numbers where negative numbers are signed 1's complement presentation	L2:Understand	CO3
6.	Multiply each of the following pairs of signed 2's complement numbers using the Booth multiplication and n- bit multipliers. In each case assume that A is multiplicand and B is multiplier. (i) A=010111 and B=110110. (ii) A=110011 and B=101100	L4:Analyse	CO1
7.	Discuss about the IEEE standard for binary floating point arithmetic	L2:Understand	CO2
8.	Draw the flowchart for divide operation and explain	L2:Understand	CO3
9.	Draw and explain the one stage decimal arithmetic unit	L2:Understand	CO3
10.	**Explain in detail about the derivation of BCD adder	L2:Understand	CO3

UNIT-4

Short Answer Questions-

S.NO	QUESTION	BLOOMS Taxonomy	Course Outcome
1.	What is DMA?	L2:Understand	CO2
2.	What is the need of IO Interface?	L2:Understand	CO2
3.	Define Priority Interrupt?	L1:Remember	CO3



4.	List out any 5 IO Devices?	L1:Remember	CO3
5.	What are peripheral devices? Give a note on video monitors.	L2:Understand	CO2

Long Answer Questions-

S.NO	QUESTION	BLOOMS Taxonomy	Course Outcome
1.	What is asynchronous data transfer? Explain the different types of Asynchronous data transfer techniques.	L2:Understand	CO2
2.	Explain in detail floating point arithmetic operations with examples.	L2:Understand	CO3
3.	What is IOP? Explain the communication between IOP and CPU.	L2:Understand	CO2
4.	Explain the following data transfer modes/techniques. a)Program Controlled IO b)Interrupt Initiated IO	L2:Understand	CO2
5.	Write a note on memory hierarchy with the neat diagram.	L2:Understand	CO3
6.	Consider a cache consisting of 256 blocks of 8 words each, for a total of 2048 words, and assume that the main memory is addressable by a 16-bit address. The main memory has 64K words which are divided into 8192 blocks of 8 words each. Find the number of bits in Tag, Block and Word Field of the main memory address for direct mapping scheme.	L4: Analyse	CO1
7.	Explain in detail about DMA operation with neat diagram	L2:Understand	CO2
8.	Describe in brief the different modes by which data transfer can take place between a computer unit and its I/O devices. What is the difference between synchronous and asynchronous data transfer?	L1: Remember	CO3



9.	Explain in detail about Cache memory mechanisms	L2:Understand	CO2
10.	Explain in detail about Associative memory mechanisms	L2:Understand	CO2

UNIT-5

Short Answer Questions-

S.NO	QUESTION	BLOOMS Taxonomy	Course Outcome
1.	List out the memory hierarchy?	L1:Remember	CO3
2.	What is associative memory?	L2:Understand	CO2
3.	What is the need of Cache Memory?	L1:Understand	CO2
4.	Define a Pipeline? Give an example.	L2:Remember	CO3
5.	What is inter process arbitration?	L2:Understand	CO3

Long Answer Questions-

S.NO	QUESTION	BLOOMS Taxonomy	Course Outcome
1.	Explain the different types of Pipeline techniques.	L2:Understand	CO3
2.	What is mean by IPC. Explain the Concurrency & Synchronization with IPC?	L2:Understand	CO3
3.	What is Multiprocessors? Explain in detail .	L1:Remember	CO4
4.	List out Cache mapping techniques and Explain all the mapping techniques?	L2:Understand	CO3
5.	Define Auxiliary memory ? Explain with neat diagram	L2:Understand	CO2
6.	Explain in detail about the RISC Characteristics	L2:Understand	CO3
7.	Explain in detail about the CISC Characteristics	L2:Understand	CO3
8.	Explain in detail about the Instruction Pipeline	L2:Understand	CO3
9.	List the Characteristics of Multiprocessors Explain in detail about the Interconnection structures of Multiprocessor	L4:Analyse	CO2
10.	Explain in detail about the Interprocessor arbitration	L2:Understand	CO3



OBJECTIVE QUESTIONS:

UNIT-I

1. The register that includes the address of the memory unit is termed as the ____
 - a) MAR
 - b) PC
 - c) IR
 - d) None of these
2. Which is the operation that a computer performs on data that put in register?
 - a) Register transfer
 - b) Arithmetic
 - c) Logical
 - d) All of these
3. Which micro operations carry information from one register to another?
 - a) Register transfer
 - b) Arithmetic
 - c) Logical
 - d) All of these
4. The 'heart' of the processor which performs many different operations _____.
 - a) Arithmetic and logic unit
 - b) Motherboard
 - c) Control Unit
 - d) Memory
5. Operation of memory transfer are -----.
 - a) Read
 - b) Write
 - c) Both
 - d) None
6. In memory read the operation puts memory address on to a register known as
 - a) PC
 - b) ALU
 - c) MAR
 - d) All of these
7. Which operation is binary type, and is performed on bits string that is placed in register?
 - a) Logical micro operation
 - b) Arithmetic micro operation
 - c) Both
 - d) None
8. Which operation is extremely useful in serial transfer of data?
 - a) Logical micro operation
 - b) Arithmetic micro operation
 - c) Shift micro operation
 - d) None of these
9. _____ is a command given to a computer to perform a specified operation on some given data:
 - a) An instruction
 - b) Command
 - c) Code
 - d) None of these
10. An instruction is guided by _____ to perform work according:
 - a) PC



- b) ALU
- c) Both a and b
- d) CPU

Fill in the Blanks

11. During the execution of the instructions, a copy of the instructions is placed in the _____

Ans: Cache

12. A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____

Ans: Pipe-lining

13. When Performing a looping operation, the instruction gets stored in the _____

Ans: Cache

14. The main virtue for using single Bus structure is _____

Ans: Cost effective connectivity and ease of attaching peripheral devices

15. To extend the connectivity of the processor bus we use _____

Ans: PCI bus

Unit – II

1. A machine language instruction format consists of

- a) Operand field
- b) Operation code field
- c) Operation code field & operand field
- d) none of the mentioned

2. What does the hardwired control generator consist of?

- a) Decoder/encoder
- b) Condition codes
- c) Control step counter
- d) All of the mentioned

3. The name hardwired came because the sequence of operations carried out is determined by the wiring.

- a) True
- b) False

4. The instruction format 'register to register' has a length of.

- a) 2 bytes
- b) 1 byte
- c) 3 bytes
- d) 4 bytes

5. The instruction "JUMP" belongs to.

- a) sequential control flow instructions
- b) control transfer instructions
- c) branch instructions
- d) control transfer & branch instructions

6. The part of a processor which contains hardware necessary to perform all the operations required by a computer:

- a) Data path
- b) Controller
- c) Registers
- d) Cache



7 What does MAR stand for?

- a) Main Address Register
- b) Memory Access Register
- c) Main Accessible Register
- d) Memory Address Register

8 If the control signals are generated by combinational logic, then they are generated by a type of _____ controlled unit.

- a) Micro programmed
- b) Software
- c) Logic
- d) Hardwired

9. A set of microinstructions for a single machine instruction is called _____.

- a) Program
- b) Command
- c) Micro program
- d) Micro command

10 In the case of, Zero-address instruction method the operands are stored in _____.

- a) Registers
- b) Accumulators
- c) Push down stack
- d) Cache

Fill in the Blanks

11.The _____ micro operator can be used to selective set bit of a register

12.The transfer of information from a memory word to the outside environment is called a _____

13.The Data Register sometimes called a _____ register

14.The addressing mode/s, which uses the PC instead of a general purpose register is _____

15.In the following indexed addressing mode instruction, MOV 5(R1),LOC the effective address is _____ Ans: $E=5+[R1]$

16.The method of accessing the I/O devices by repeatedly checking the status flags is _____.

Ans: Status flags

17.The method of accessing the I/O devices by repeatedly checking the status flags is _____.

Ans: a) Program-controlled I/O

Unit - III

1. Which of the following is not a decimal number?

- a) 114
- b) 43.47
- c) 99.9A
- d) 10101

2. A computer language that is written in binary codes only is _____.

- a) Machine language
- b) C
- c) C#
- d) pascal

3. The input hexadecimal representation of 1110 is _____.



- a) 0111
 - b) E
 - c) 15
 - d) 14
4. Convert the binary equivalent 10101 to its decimal equivalent.
- a) 21
 - b) 12
 - c) 22
 - d) 31
5. Which of the following is not a binary number?
- a) 1111
 - b) 101
 - c) 11E
 - d) 000
6. Which of the following is the correct representation of a binary number?
- a) (124)₂
 - b) 1110
 - c) (110)₂
 - d) (000)₂
7. What could be the maximum value of a single digit in an octal number system?
- a) 8
 - b) 7
 - c) 6
 - d) 5
8. The maximum number of bits sufficient to represent an octal number in binary is _____.
- a) 4
 - b) 3
 - c) 7
 - d) 8
9. The binary number 111 in octal format is _____.
- a) 6
 - b) 7
 - c) 8
 - d) 5
10. The octal equivalent of the binary number (0010010100)₂ is _____.
- a) 422
 - b) 242
 - c) 224
 - d) 226

Fill in the Blanks

11. The pipelining process is also called as _____.
Ans: Assembly line operation
12. The fetch and execution cycles are interleaved with the help of _____.
Ans: Clock
13. To increase the speed of memory access in pipelining, we make use of _____.
Ans: Cache
- _____ have been developed specifically for pipelined systems.



Ans: Optimizing compilers

14. The clock rate of the processor can be improved by _____

Ans: Reducing the amount of processing done in one step By using the overclocking method

UNIT – IV

1. Any electronic holding place where data can be stored and retrieved later whenever required is _____.

- a) memory
- b) drive
- c) disk
- d) circuit

2. Which of the following is the fastest means of memory access for CPU?

- a) Registers
- b) Cache
- c) Main memory
- d) Virtual Memory

3. The memory implemented using the semiconductor chips is _____.

- a) Cache
- b) Main
- c) Secondary
- d) Registers

4. Size of the _____ memory mainly depends on the size of the address bus.

- a) Main
- b) Virtual
- c) Secondary
- d) Cache

5. What is the high speed memory between the main memory and the CPU called?

- a) Register Memory
- b) Cache Memory
- c) Storage Memory
- d) Virtual Memory

6. Whenever the data is found in the cache memory it is called as _____.

- a) HIT
- b) MISS
- c) FOUND
- d) ERROR

7. LRU stands for _____.

- a) Low Rate Usage
- b) Least Rate Usage
- c) Least Recently Used
- d) Low Required Usage

8. When the data at a location in cache is different from the data located in the main memory, the cache is called _____.

- a) Unique
- b) Inconsistent
- c) Variable
- d) Fault

9. Which of the following is not a write policy to avoid Cache Coherence?



- a) Write through
- b) Write within
- c) Write back
- d) Buffered write

10. In _____ mapping, the data can be mapped anywhere in the Cache Memory.

- a) Associative
- b) Direct
- c) Set Associative
- d) Indirect

Fill in the Blanks

11. Which representation is most efficient to perform arithmetic operations on the numbers?

Ans: 2'S complement

12. The processor keeps track of the results of its operations using a flags called _____

Ans: Conditional code flags

13. The register used to store the flags is called as _____

Ans: Status register

14. The Flag 'V' is set to 1 indicates that,

Ans: The operation has resulted in an overflow

15. The most efficient method followed by computers to multiply two unsigned numbers is _____

Ans: Bit pair recording of multipliers

UNIT - V

1. The CISC stands for _____.

- a) Computer Instruction Set Compliment
- b) Complete Instruction Set Compliment
- c) Computer Indexed Set Components
- d) Complex Instruction set computer

2. The computer architecture aimed at reducing the time of execution of instructions is _____.

- a) CISC
- b) RISC
- c) ISA
- d) ANNA

3. The Sun micro systems processors usually follow _____ architecture.

- a) CISC
- b) ISA
- c) ULTRA SPARC
- d) RISC

4. The iconic feature of the RISC machine among the following is _____.

- a) Reduced number of addressing modes
- b) Increased memory size
- c) Having a branch delay slot
- d) All of the mentioned

5. Both the CISC and RISC architectures have been developed to reduce the _____.

- a) Cost
- b) Time delay



- c) Semantic gap
 - d) All of the mentioned
6. To increase the speed of memory access in pipelining, we make use of _____.
a) Special memory locations
b) Special purpose registers
c) Cache
d) Buffers
7. When the processor executes multiple instructions at a time it is said to use _____.
a) single issue
b) Multiplicity
c) Visualization
d) Multiple issues
8. Which of the following architecture is/are not suitable for realizing SIMD?
a) Vector Processor
b) Array Processor
c) Von Neuman
d) All of the above
9. In super-scalar processors, _____ mode of execution is used.
a) In-order
b) Post order
c) Out of order
d) None of the mentioned
10. _____ have been developed specifically for pipelined systems.
a) Utility software
b) Speed up utilities
c) Optimizing compilers
d) None of the mentioned

Fill in the Blanks

11. In multiple Bus organisation, the registers are collectively placed and referred as _____

Ans: Register file

12. The main advantage of multiple bus organisation over a single bus is _____

Ans: Reduction in the number of cycles for execution

GATE: (If applicable)

1. Consider a two-level cache hierarchy with **L1** and **L2** caches. An application incurs **1.4** memory accesses per instruction on average. For this application, the miss rate of **L1** cache is **0.1**; the **L2** cache experiences, on average, **7** misses per 1000 instructions. The miss rate **L2** expressed correct to two decimal places is _____. (GATE 2107)
2. A processor can support a maximum memory of 4GB, where the memory is word-addressable (a word consists of two bytes). The size of the address bus of the processor is at least bits. (GATE2016)
3. The width of the physical address on a machine is 40 bits. The width of the tag field in a 512 KB 8-way set associative cache is _____ bits. (GATE 2016)
4. A processor has 40 distinct instructions and 24 general purpose registers. A 32-bit instruction word has an opcode, two register operands and an immediate operand. The number of bits available for the immediate operand field is _____. (GATE 2016)
5. Consider a non-pipelined processor with a clock rate of 2.5 gigahertz and average cycles per instruction of four. The same processor is upgraded to a pipelined processor with five



stages; but due to the internal pipelined delay, the clock speed is reduced to 2 gigahertz. Assume that there are no stalls in the pipeline. The speed up achieved in this pipelined processor is _____. (GATE 2016)

WEBSITES:

<http://www.geeksforgeeks.org/computer-organization-and-architecture-gg/>

<https://www.cs.virginia.edu/c++programdesign/slides/pdf/bw01.pdf>

https://www.tutorialspoint.com/computer_organization/index.asp

<https://sites.google.com/site/uopcog/>

Seminar Topics:

- 1) Pentium IV Architecture
- 2) SIMD
- 3) High performance Architecture
- 4) Parallel Computer Architecture